

A Wide Range Temperature Stable Integrated Current Reference

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Abstract

A current reference integrated circuit was built in a 2 micron CMOS process based on SIMOX technology, without the need of external trimming, to provide 19.5 μA . The overall error was less than $\pm 1\%$ ($< 67 \text{ ppm/K}$) over 240 K temperature range from -40 to 200°C ($V_{dd} < 5 \text{ V}$, $V_{cc} > 10\text{V}$), at a power consumption of less than 1.5 mW. From -15 to 90°C the TC was $< 12 \text{ ppm/K}$, derived by higher order temperature compensation. The temperature dependence of the diode parameters is cancelled out against the temperature coefficient of the resistors. The error of the absolute current value was $\pm 5\%$ (30 circuits from two different wafers).

The circuit of 0.3 mm^2 contains only p-channel and n-channel MOS transistors, pin-diodes, and p+ resistors. It is applicable for oscillator and filter frequency stability, and for precise time delay circuits, especially in smart power and high temperature applications.

1. Introduction

A general task in designing analogue integrated circuits is to provide a current reference which is stable over temperature and over supply voltage, as for frequency stability of oscillators and filters, or for accurate time delays [1]. In most of the cases, bipolar transistors are used to achieve accurate on-chip current references [1], [2], [4], where in this work pindiods have been used only.

2. Design

Fig. 1 shows the block diagram of the circuit. A PTAT current is used to supply a diode D6 and a resistor R3 in parallel (section B). The current in the resistor depends on resistor temperature coefficient, and on the temperature dependent diode voltage drop, as well. The NTC current is mirrored from R3 by a factor k_n , and added to the PTAT current, mirrored by a factor k_p in section C to achieve a reference current I_{ref} . Practically, the schematic of the circuit, shown in Fig. 7, contains a two stage high-swing cascode to minimize the error,

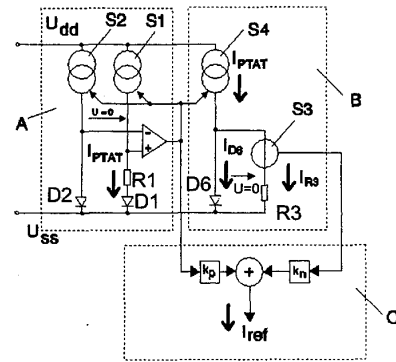


Fig.1: Block Diagram of Current Reference Circuit

caused by the swing of the supply voltage V_{dd} . The PTAT current is given by

$$I_{PTAT} = \frac{m U_T}{R1} \ln \left(\frac{A_{D1}}{A_{D2}} \right) \quad (1)$$

$$\text{and } U_T = \frac{k T}{q} \quad (2).$$

The negative temperature coefficient current (NTC) is found by

$$I_{NTC} = I_{R3} = \frac{U_{D6}}{R3} \quad (3),$$

and the temperature dependence in the Shockley model, for low emission coefficients near $m=1.0$:

$$\frac{\partial U_{D6}}{\partial T} = \frac{U_{D6}}{T} - \frac{m k}{q} \left(3 + \frac{E_{G0}}{k T} \right) \approx \frac{1}{T} \left(U_{D6}(T) - m(T) \frac{E_{G0}}{q} \right) \quad (4)$$

A resistor depends on temperature by

$$R = R_N (1 + k_R \Delta T) \quad (5),$$

when it's quadratic temperature coefficient is neglected. In this case,

$$T_N = 343 \text{ K} = 70^\circ\text{C} \quad (6)$$

was assumed as the nominal temperature, where the constant term of the current temperature coefficient

becomes zero. The applied doping profile of silicon leads to a diode nominal built-in potential of U_{DN} ,

$$U_{DN} = \frac{k T_N}{q} \ln \left(\frac{N_A N_D}{n_i^2} \right) \quad (6a)$$

which was 655 mV. Considering the current density being large enough to meet the "linear" region of a diode shown in Fig.3, diode D1 was designed to have at least a current density of more than 50 nA/ μm^2 . To achieve the constant term temperature compensation, equations (1) and (3) have to be differentiated, including the addition factors k_n and k_p , and set to be equal. Taylor's series, applied to the expression $1/T$, considering the first two elements, as well as other simplifications deliver the results for the currents to be added:

$$\frac{\partial I_{NTC}}{\partial T} \approx \frac{k_n}{T_N} m(T) \left(1 - \frac{\Delta T}{T_N} \right) \left(\frac{U_{D6}(T)}{m(T)} - \Delta U_{Si} \right) \frac{1}{R3_N (1 + k_R \Delta T)^2} < 0 \quad (7)$$

$$\frac{\partial I_{PTAT}}{\partial T} \approx \frac{k_p}{T_N} m(T) U_{TN} \ln \left(\frac{A_{D1}}{A_{D2}} \right) \frac{1 - k_R T_N}{R1_N (1 + k_R \Delta T)^2} > 0 \quad (8)$$

From (7) and (8), the R3/R1 resistance ratio was found:

$$\frac{R3_N}{R1_N} = \frac{k_n}{k_p} \frac{\Delta U_{Si} - \frac{U_{D6}(T_N)}{m(T_N)}}{U_{TN} \ln \left(\frac{A_{D1}}{A_{D2}} \right) (1 - k_R T_N)} \quad (9)$$

While $m(T_N)=1.27$, ΔU_{Si} had an empirical constant value stabilized by the technology, considering that neither the Shockley model ($m=1$) is applicable, nor the Sah-Noyce-Shockley model ($m=2$).

$$\Delta U_{Si} \approx 938 \text{ mV} < \frac{E_{G0, Si}}{q} = 1.12 \text{ V} \quad (10)$$

As to be seen, the temperature coefficient of $U_{D6}(T)$ in (7) can be influenced by the temperature itself, and by the current density, which increases with temperature, while $I_{PTAT} - I_{NTC}$ is flowing through D6 (see Fig. 5). In a second step, the cancellation of the first order term $\Delta T/T_N$ in (7), appearing as the quadratic temperature dependence, is achieved by choosing the right length of the intrinsic area from Fig. 4 for the diodes. Fig. 5 illustrates the compensation effect of the current density at 27°C, which is also nearly independent from the diodes area at any chosen temperature. The schematic of the complete circuit is shown in Fig. 7. Additionally, a voltage reference is included to provide a constant voltage of 1.19 V in this case,

which may be used in analogue circuit applications. Former high-temperature suited ICs are based on this reference, which has been used as a non-trimming on-chip voltage reference, e.g. in [3].

3. Measurement results

Fig. 2 shows current measurements at $V_{CC}=10\text{V}$, of the external circuits, supplied by the current reference. The external circuit was supplied by V_{CC} , while the current reference circuit of Fig. 1 was supplied by V_{DD} . The errors in Fig. 2 would become larger due to the influence of the saturation region of the drain-source voltage, if V_{CC} would be decreased. The chip micrograph, shown in Fig. 6, includes a chip area of 0.3 mm^2 .

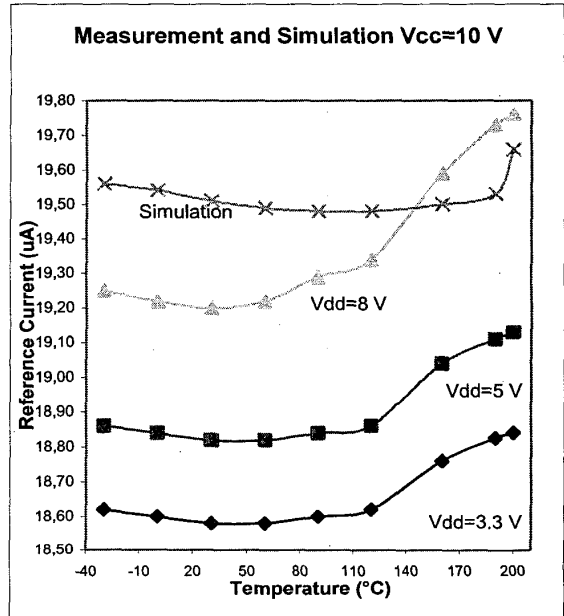


Fig. 2: Measurement and Simulation of Temperature Stability ($V_{DD} < V_{CC}$)

Current Density ($\text{A}/\mu\text{m}^2$)

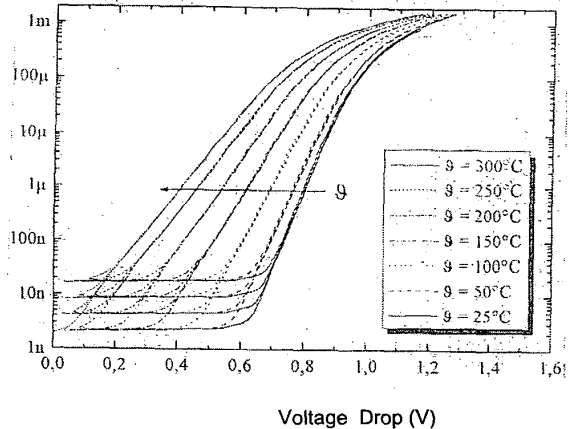


Fig. 3: Voltage-Current Characteristics of Pindiodes

Emission Coefficient m_e

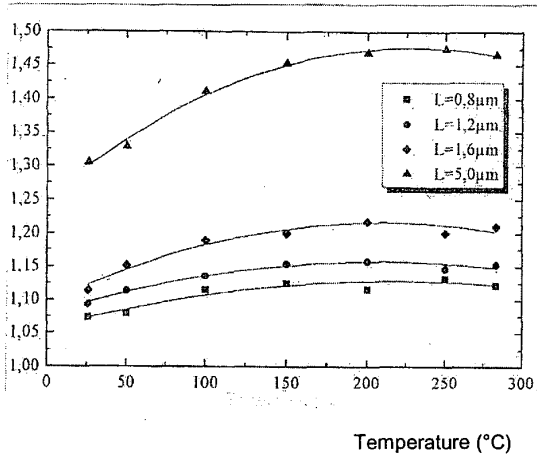


Fig. 4: Temperature Dependency of Emission Coefficient

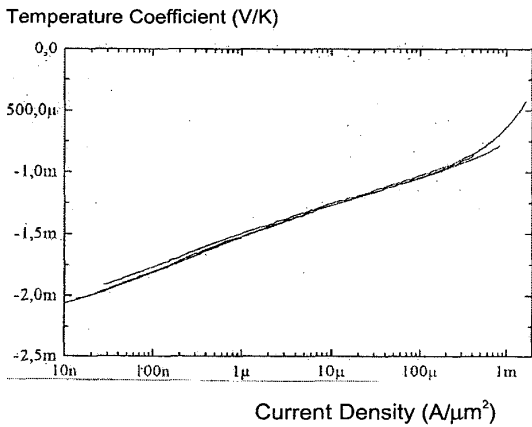


Fig. 5: Temperature Coefficient of Forward Voltage Drop (for 6 Diodes of different Width)

4. Conclusions

The circuit will be applied for power control integrated circuits, where non-trimming current sensors are desired to optimise the costs. The reported circuit is suited to work at very low voltages when transferred to large scaled technologies in the future, as in low voltage memory circuits, or in battery operated low power circuits, where sub-1-V operation is required.

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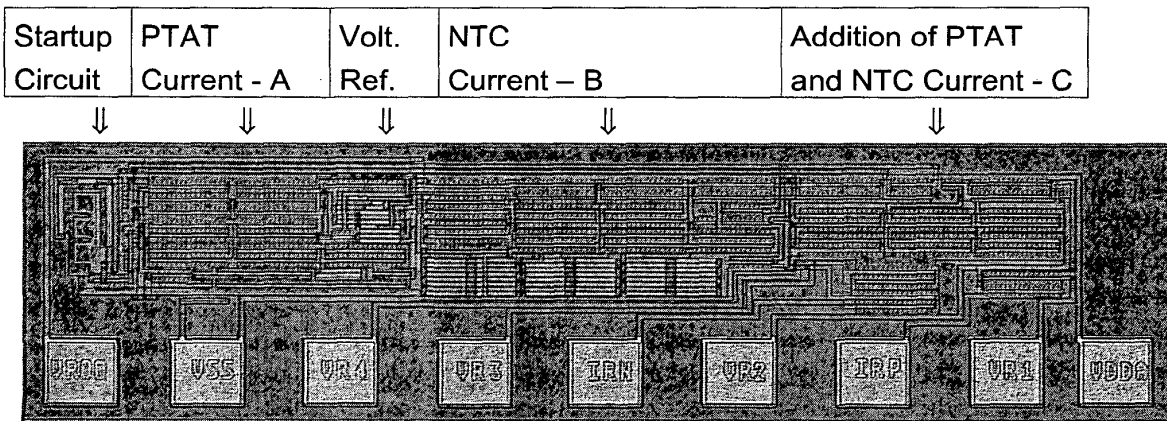


Fig. 6: Chip Micrograph

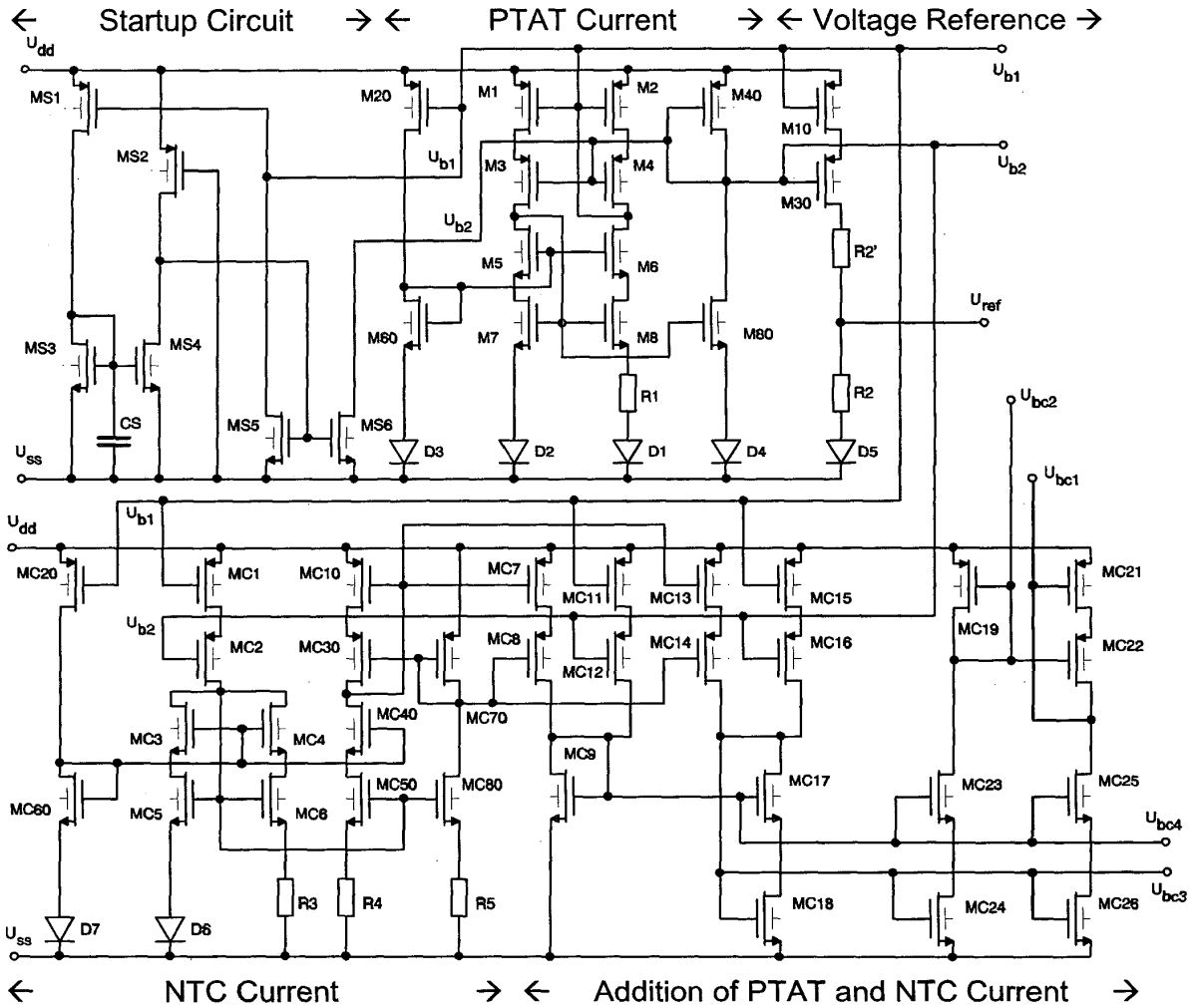


Fig. 7: Schematic of Current Reference Circuit

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